IN THE SPECIFICATION

Please replace paragraph [0032] with the following amended paragraph:

[0032] After the second differential comparator 32 is driven by the trigger signal, the input signals each with an input voltage of 0 to 2Volt are received by the second differential receiving circuit including the pre-amplifier receiving circuit 321 (having transistors T6-T11) and the main receiving circuit 322 (having transistors T3-T5), the received voltages are amplified by the second differential comparator 32 further including the shared active load 312, which is electrically connected to the main ~~differential~~ receiving circuit 322 to form a second operational amplifier (including elements 322, 312), and the output voltages are produced and output through the output circuit 33.

Please replace paragraph [0034] with the following amended paragraph:

[0034] The pre-amplifier ~~differential~~ receiving circuit 321 includes a set of NMOSs (T8 and T11) and PMOSs (T9- T10) with two receiving terminals (IN+ and IN-) and a level shift circuit 3211 (having transistors T6-T7) so as to avoid the floating and to gain the cumulative effect. Regarding the PMOSs, the output voltage is output at a higher level of V_{dd} when the voltage values of IN+ > IN-. Regarding the PMOSs, the output voltage is output at a lower level of 0 when the voltage values of IN+ < IN-. The output voltage mentioned above is varied

according to which one of the two values of IN+ and IN- is relatively larger or smaller.

Please replace paragraph [0035] with the following amended paragraph:

[0035] Please refer to Fig. 4, the pre-amplifier ~~differential~~ receiving circuit 321 will be shut down when the receiving voltages of IN+ and IN- are too high. Therein, the level shift circuit 3211 can be employed to amplify the receiving input signals initially and to shut down the two receiving terminals when the stop signal is generated by the detecting circuit 30.